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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/776,139	02/09/2004	Ming-Tung Shen	08688.0128USD1	3033

23552 7590 07/27/2005

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EXAMINER	
DOAN, THERESA T	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/776,139	SHEN, MING-TUNG	
	Examiner	Art Unit	
	Theresa T. Doan	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 20-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 20-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/407,204.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/09/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The preliminary amendment filed 02/09/04 has being acknowledged and entered. By this amendment claims 2-19 are cancelled and claims 1 and 20-24 are pending in the application.

Information Disclosure Statement

2. The prior art documents submitted by applicant in the Information Disclosure Statement filed on 02/09/04, have all been considered and made of record (note the attached copy of form PTO-1449).

Drawings

3. The drawings, filed on 02/09/04, are accepted.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical

Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 1 and 22-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Gelsomini et al. (US. Pat. 6,278,616).

Regarding claim 1, Gelsomini (Fig. 1) discloses a semiconductor chip module comprising:

a chip-mounting member 11 having opposite first and second surfaces (11a,11b), a set of circuit traces 12 (column 5, lines 1-4) disposed on the first surface 11a of the chip-mounting member 11, and a plurality of plated through holes 21 that extend through the first and second surfaces (11a,11b) and that are electrically connected to the circuit traces 12, the chip-mounting member 11 being formed with a first opening 15 that extends through the first and second surfaces (11a,11b) thereof (see Fig. 1 labeled by the Examiner below);

a semiconductor chip 10 (column 5, lines 9-11) having a pad mounting surface with a plurality of contact pads 18 provided thereon;

a dielectric tape member 14 (column 5, lines 15-17) for bonding adhesively the pad mounting surface of the semiconductor chip 10 on the second surface 11b of the chip-mounting member 11, the dielectric tape member 14 being formed with a second opening that is registered with the first opening 15 for access to the contact pads 18 of the semiconductor chip 10 (see Fig. 1 labeled by the Examiner below);

a conductor unit including a plurality of wires 17 for connecting electrically the contact pads 18 of the semiconductor chip 10 and the circuit traces 12 on the first surface 11a of the chip-mounting member 11; and

a plurality of solder balls 16 disposed on one of the first and second surfaces 11a and 11b of the chip-mounting member 10, each of the solder balls 16 being aligned with and being connected to a respective one of the plated through holes 21 in the chip-mounting member 11 (column 5, lines 26-30).

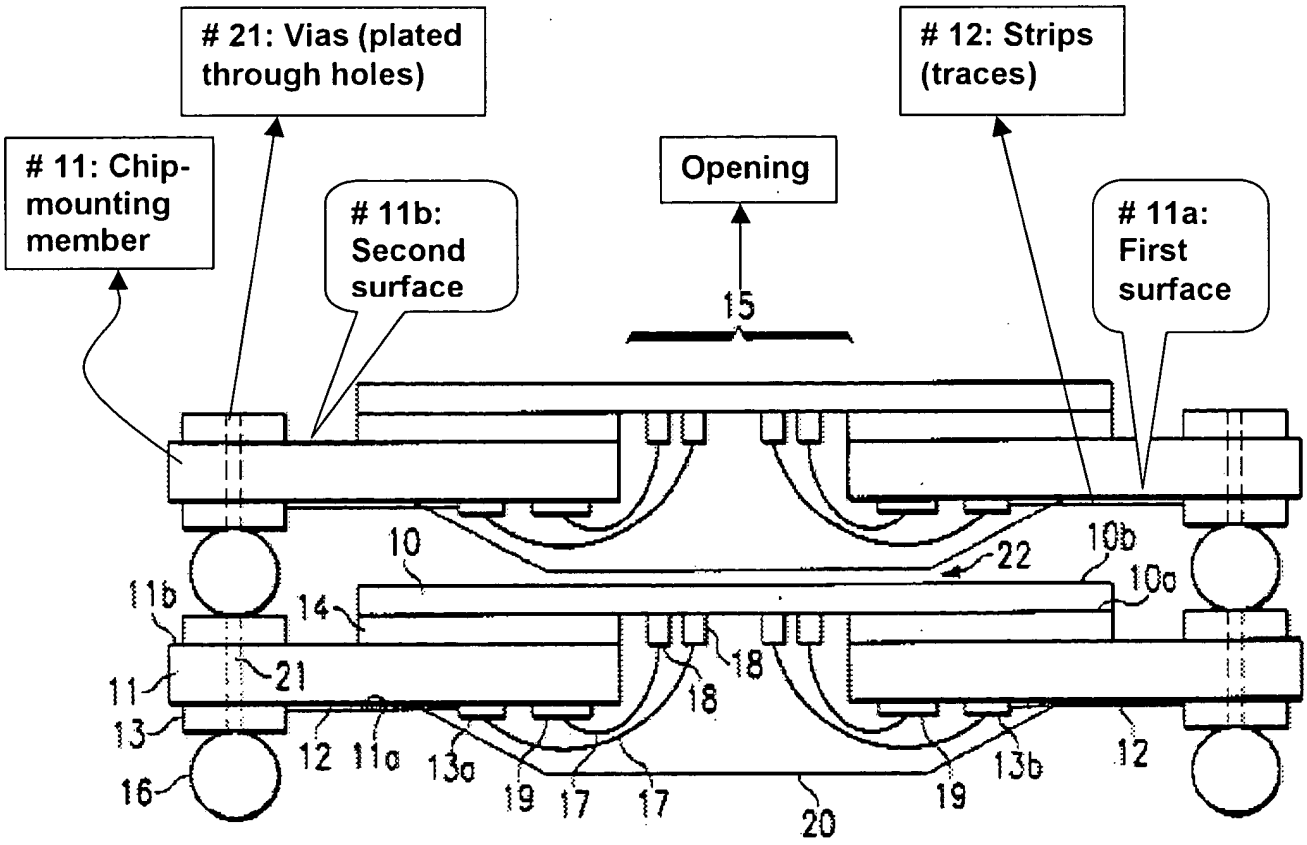
21: Vias (plated through holes)
12: Strips (traces)
11: Chip-mounting member
Opening
11b: Second surface
11a: First surface
15
10
22
10b
10a
11b
14
18
18
11
21
13
12
11a
13a
19
17
17
20
19
13b
12
16

FIG. 1

Regarding claim 22, Gelsomini (Fig. 1) further discloses that an encapsulation layer 20 provided on the first surface 11a of the chip-mounting member 11 to enclose the pad mounting surface of the semiconductor chip 10 and the conductor unit 17 (column 5, lines 58-61).

Regarding claim 23, Gelsomini (Fig. 1) discloses a semiconductor chip module stack, comprising:

Upper and lower semiconductor chip modules 10, each including

a chip-mounting member 11 having opposite first and second surfaces (11a,11b), a set of circuit traces 12 (column 5, lines 1-4) disposed on the first surface 11a of the chip-mounting member 11, and a plurality of plated through holes 21 that extend through the first and second surfaces (11a,11b) and that are electrically connected to the circuit traces 12, the chip-mounting member 11 being formed with a first opening 15 that extends through the first and second surfaces (11a,11b) thereof (see Fig. 1 labeled by the Examiner),

a semiconductor chip 10 (column 5, lines 9-11) having a pad mounting surface with a plurality of contact pads 18 provided thereon,

a dielectric tape member 14 (column 5, lines 15-17) for bonding adhesively the pad mounting surface of the semiconductor chip 10 on the second surface 11b of the chip-mounting member 11, the dielectric tape member 14 being

formed with a second opening that is registered with the first opening 15 for access to the contact pads 18 of the semiconductor chip 10 (see Fig. 1 labeled by the Examiner),

a conductor unit including a plurality of wires 17 for connecting electrically the contact pads 18 of the semiconductor chip 10 and the circuit traces 12 on the first surface 11a of the chip-mounting member 11, and

a plurality of solder balls 16 disposed on one of the first and second surfaces 11a and 11b of the chip-mounting member 10, each of the solder balls 16 being aligned with and being connected to a respective one of the plated through holes 21 in the chip-mounting member 11 (column 5, lines 26-30);

wherein the upper and lower semiconductor chip modules 10 are interconnected by the solder balls 16 on the chip-mounting member 11 of one of the upper and lower semiconductor chip modules 10 and the plated through holes 21 in the chip-mounting member 11 of the other one of the upper and lower semiconductor chip modules 10 (see Fig. 1).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gelsomini et al. (US. Pat. 6,278,616) as applied to claim 1 above, in view of Yew et al. (US. Pat. 6,049,129).

Gelsomini does not disclose that the peripheral portion of the semiconductor chip 10 is provided with an epoxy resin layer for bonding the chip to the chip-mounting member 11.

However, Yew (Fig. 6) teaches a semiconductor chip module having a semiconductor chip 50 mounted to the second surface of a chip-mounting member 70, and the peripheral portion of the semiconductor chip 50 is provided with an epoxy resin layer 90 (column 7, lines 26-35) for bonding the chip to the chip-mounting member 70. Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to provide an epoxy resin at the peripheral portion of the semiconductor chip 10 of Gelsomini because the epoxy resin is an adhesive material which has high strength and flexibility characteristics (as taught by Yew, column 7, lines 26-35) to strengthen bonding of the semiconductor chip with the second surface of the chip-mounting member.

8. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gelsomini et al. (US. Pat. 6,278,616) as applied to claim 1 above, in view of Akram (US. Pub. 2002/0060369).

Gelsomini does not disclose a heat dissipating plate secured on a back surface of the semiconductor chip 10.

However, Akram (Fig. 6) teaches a semiconductor chip module comprising a semiconductor chip 62 bonding to a chip-mounting member 52, the semiconductor chip 62 having a heat dissipating surface 66 that is opposite to the pad mounting surface 58 and that has a heat dissipating plate 80 secured thereon, to improve dissipation of heat from chip 62 (paragraph [0040]).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to attach a heat dissipating plate on the back or on the heat dissipating surface of the semiconductor chip 10 of Gelsomini because such forming of the heat dissipating plate on the heat dissipating surface of the semiconductor chip 10 would improve dissipation of heat from chip, as taught by Akram (paragraph [0040]).

9. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gelsomini et al. (US. Pat. 6,278,616) as applied to claim 23 above, in view of Lin (US. Pat. 6,093,969).

As discussed in details above, Gelsomini (Fig. 1) discloses a first semiconductor chip module made of board-on-chip BGA having the solder balls 16 provided on the first surface of the chip-mounting member 11. Gelsomini (Fig. 2) further discloses a second semiconductor chip module made of board-on-chip BGA having the solder balls 106 provided on the second surface of the chip-mounting member 101, and having a plurality of plated through holes 121 that extend through the first and second surfaces of the chip mounting member 101.

Gelsomini does not disclose that the solder balls 16 of the first semiconductor chip module of Fig. 1 are connected to the plated through holes 121 of the second semiconductor module of Fig. 2 at the first surface of the chip mounting member 101 to form a semiconductor chip module stack.

However, Lin (Fig. 3) teaches a semiconductor chip module stack comprising upper and lower semiconductor modules, each made of board-on-chip BGA. The upper semiconductor module 120-2 having the solder balls 130-2 provided on the first surface of the upper chip-mounting member 103-2, and the lower semiconductor module 120-1 having the solder balls (not labeled) provided on the second surface of the lower chip mounting member 103-1. The solder balls 130-2 of the upper semiconductor chip module 120-2 are aligned with and are connected to the plated through holes 106 in the lower chip mounting member 103-1 of the lower semiconductor chip module 120-1 at the first surface of the lower chip mounting member 103-1.

Accordingly, in view of teachings of Lin, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the semiconductor chip module stack of Gelsomini by stacking the semiconductor chip module of Fig. 1 on the semiconductor chip module of Fig.2 and having the solder balls 16 of the semiconductor chip module of Fig. 1 being aligned with and being connected to the plated through holes 121 in the chip mounting member 101 of the semiconductor chip module of Fig. 2 at the bonding pads 103 or at the first surface of the mounting member 101 because such stacking of the semiconductor chip modules would provide

a face-to-face stacked chip module for improving the packing density and also improving the signal transmission, as taught by Lin (column 5, lines 29-33).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Theresa T. Doan whose telephone number is (571) 272-1704. The examiner can normally be reached on Monday to Friday from 7:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, WAEL FAHMY can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Theresa Doan
July 22, 2005.